ABSTRACT

The invention relates to a circuit arrangement with two or more circuit sections, which cooperate through a data transfer device. The invention solves the problem of double area expenditure for two memory devices for each receiver, in that the data bus itself takes over the role of one of these memory devices, namely that of the memory device functioning as master. For this it is only necessary to integrate a single memory device on the data bus, which takes over the role of the no longer needed memory device for each data receiver. By saving the memory device associated with each receiver, the semiconductor chip area needed for communication buses can be optimized.